



U.S. Patent Application No.: 10/716,595

Attorney Docket No.: 57941.000062

Client Reference No.: RA001.2003.1.C.US

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Application of:

Michael Farmwald, et al.

Appln. No.: 10/716,595

Filed: November 20, 2003

For: MEMORY DEVICE AND METHOD FOR  
OPERATING SAME

:  
: Group Art Unit: 2827  
:  
: Examiner: Tan Nguyen  
:  
: Confirmation No.: 7213  
:  
: Customer No.: 21967  
:  
:

Mail Stop Amendment  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**INFORMATION DISCLOSURE STATEMENT**

Sir:

In accordance with the duty under 37 C.F.R. § 1.56 of each individual associated with the filing and prosecution of the above-identified patent application (hereinafter, "associated individuals") to disclose all information known to that individual to be material to patentability, Applicants hereby submit attached Form PTO-1449 (modified) listing cited references. This submission is made in accordance with 37 C.F.R. §§ 1.97 and 1.98 and M.P.E.P. § 609.

Please note that the vast majority of the cited references were recently identified by parties contesting the validity of U.S. patents related to above-identified patent application in two separate proceedings before the U.S. District Court for the

Northern District of California, namely Rambus Inc. v. Samsung Electronics Co., Ltd. et al. (Case No. C 05-02298 RMW) and Hynix Semiconductor Inc. et al. v. Rambus Inc. (Case No. CV 00-20905 RMW). To avoid overburdening the Examiner as much as possible, Applicants have checked to make sure that the cited references have not been previously cited in the above-identified patent application.

The cited references, while believed to be of some relevance, are not necessarily considered to teach or suggest any aspect of the invention described and claimed in the above-identified patent application. Applicants hereby expressly reserve the right to swear behind the effective dates of any of the cited references. Applicants further reserve the right to question the relevance, materiality, and/or prior art status of any of the cited references in whole, in part, or in combination, subsequent to the filing of this information disclosure statement. This information disclosure statement is also not to be construed as a representation that a search has, or has not, been conducted or that no better art exists. Rather, this information disclosure statement discloses only the references of which the associated individuals are aware.

The Examiner is respectfully requested to consider each of the cited references, to indicate such consideration by

initialing in the space provided next to each cited reference on the enclosed Form PTO-1449 (modified), to sign the initialed Form PTO-1449 (modified), and to return a copy of the same with the next communication to the Applicants.

In accordance with 37 C.F.R. § 1.98(a), only copies of the cited references which are not U.S. patents or U.S. patent application publications are being submitted herewith. However, copies of the cited references which are U.S. patents or U.S. patent application publications will be submitted at the request of the Examiner. In considering these cited references, it may be noted by the Examiner that certain of the references may contain markings, underlinings, and/or other notations. These markings, underlinings, and/or other notations are not to be construed as drawing the Examiner's attention either to selected parts or away from other parts of these cited references. Any such markings were either present on the copies of these cited references when obtained by the associated individuals, or were made thereon during the study of these cited references by the associated individuals.

In accordance with 37 C.F.R. § 1.97(b), this information disclosure statement is being filed (i) within three months of the filing date of the above-identified patent application; (ii) within three months of the date upon which the above-identified

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patent application entered the national stage as set forth in 37 C.F.R. § 1.491; (iii) before the mailing date of a first Office Action on the merits for the above-identified patent application; or (iv) before the mailing date of a first Office Action after the filing of a request for continued examination under 37 C.F.R. § 1.114. Accordingly, no statement or fee is required.

Please charge any shortage in fees due in connection with the filing of this communication to Deposit Account No. 50-0206, and please credit any excess fees to such deposit account.

Respectfully submitted,

Hunton & Williams LLP

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Date: June 29, 2006

Substitute for form 1449A/PTO  <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> <i>(use as many sheets as necessary)</i>		<b>Application Number</b>	<b>10/716,595</b>
		<b>Filing Date</b>	<b>November 20, 2003</b>
		<b>First Named Inventor</b>	<b>Michael Farnwald</b>
		<b>Art Unit</b>	<b>2827</b>
		<b>Examiner Name</b>	<b>Tan Nguyen</b>
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**U.S. PATENT DOCUMENTS**

*Examiner Initials	Cite No.	DOCUMENT NUMBER Number - Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1.	US- 3,633,166	01-04-1972	Picard	
	2.	US- 3,740,723	06-19-1973	Beausoleil, et al.	
	3.	US- 3,758,761	09-11-1973	Henrion	
	4.	US- 3,882,470	05-06-1975	Hunter	
	5.	US- 3,924,241	12-02-1975	Kronies	
	6.	US- 3,972,028	07-27-1976	Weber, et al.	
	7.	US- 3,975,714	08-17-1976	Weber, et al.	
	8.	US- 3,983,537	09-28-1976	Parsons, et al.	
	9.	US- 4,007,452	02-08-1977	Hoff, Jr.	
	10.	US- 4,038,648	07-26-1977	Chesley	
	11.	US- 4,047,246	09-06-1977	Kerllenevich, et al.	
	12.	US- 4,048,673	09-13-1977	Hendrie, et al.	
	13.	US- 4,191,996	03-04-1980	Chesley	
	14.	US- 4,231,104	10-28-1980	St. Clair	
	15.	US- 4,234,934	11-18-1980	Thorsrud	
	16.	US- 4,249,247	02-03-1981	Patel	
	17.	US- 4,263,650	04-21-1981	Bennett, et al.	
	18.	US- 4,286,321	08-25-1981	Baker, et al.	
	19.	US- 4,306,298	12-15-1981	McElroy	
	20.	US- 4,322,635	03-30-1982	Redwine	
	21.	US- 4,333,142	06-01-1982	Chesley	
	22.	US- 4,337,523	06-29-1982	Hotta, et al.	
	23.	US- 4,354,258	10-12-1982	Sato	

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DATE CONSIDERED

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	24.	US- 4,355,376	10-19-1982	Gould	
	25.	US- 4,373,183	02-08-1983	Means, et al.	
	26.	US- 4,375,665	03-01-1983	Schmidt	
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	28.	US- 4,435,762	03-06-1984	Milligan, et al.	
	29.	US- 4,443,864	04-17-1984	McElroy	
	30.	US- 4,449,207	05-15-1984	Kung, et al.	
	31.	US- 4,466,127	08-14-1984	Ohgishi, et al.	
	32.	US- 4,468,738	08-28-1984	Hansen, et al.	
	33.	US- 4,470,114	09-04-1984	Gerhold	
	34.	US- 4,481,625	11-06-1984	Roberts, et al.	
	35.	US- 4,481,647	11-06-1984	Gombert, et al.	
	36.	US- 4,482,999	11-13-1984	Janson, et al.	
	37.	US- 4,488,218	12-11-1984	Grimes	
	38.	US- 4,494,186	01-15-1985	Goss, et al.	
	39.	US- 4,500,905	02-19-1985	Shibata	
	40.	US- 4,513,370	04-23-1985	Ziu, et al.	
	41.	US- 4,513,374	04-23-1985	Hooks, Jr.	
	42.	US- 4,528,661	07-09-1985	Bahr, et al.	
	43.	US- 4,566,098	01-21-1986	Gammage, et al.	
	44.	US- 4,566,099	01-21-1986	Magerl	
	45.	US- 4,571,672	02-18-1986	Hatada, et al.	
	46.	US- 4,849,937	07-18-1989	Yoshimoto	

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Substitute for form 1449A/PTO  <h2 style="text-align: center; margin: 0;">INFORMATION DISCLOSURE STATEMENT BY APPLICANT</h2> <p style="text-align: center; margin: 0;"><i>(use as many sheets as necessary)</i></p>		<b>Application Number</b> <b>10/716,595</b>	<b>Filing Date</b> <b>November 20, 2003</b>
		<b>First Named Inventor</b> <b>Michael Farnwald</b>	<b>Art Unit</b> <b>2827</b>
		<b>Examiner Name</b> <b>Tan Nguyen</b>	
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	47.	US- 4,586,167	04-29-1986	Fujishima, et al.	
	48.	US- 4,589,108	05-13-1986	Billy	
	49.	US- 4,595,923	06-17-1986	McFarland, Jr.	
	50.	US- 4,608,700	08-26-1986	Kirtley, Jr., et al.	
	51.	US- 4,616,268	10-07-1986	Shida	
	52.	US- 4,625,307	11-25-1986	Tulpule, et al.	
	53.	US- 4,633,735	01-06-1987	Sakurai, et al.	
	54.	US- 4,635,192	01-06-1987	Ceccon, et al.	
	55.	US- 4,636,986	01-13-1987	Pinkham	
	56.	US- 4,646,270	02-24-1987	Voss	
	57.	US- 4,649,516	03-10-1987	Chung, et al.	
	58.	US- 4,654,655	03-31-1987	Kowalski	
	59.	US- 4,656,605	04-07-1987	Clayton	
	60.	US- 4,660,141	04-21-1987	Ceccon, et al.	
	61.	US- 4,672,470	06-09-1987	Morimoto, et al.	
	62.	US- 4,675,813	06-23-1987	Locke	
	63.	US- 4,706,166	11-10-1987	Go	
	64.	US- 4,719,505	01-12-1988	Katznelson	
	65.	US- 4,719,602	01-12-1988	Hag, et al.	
	66.	US- 4,719,627	01-12-1988	Peterson, et al.	
	67.	US- 4,745,548	05-17-1988	Blahut	
	68.	US- 4,748,617	05-31-1988	Drewlo	
	69.	US- 4,750,839	06-14-1988	Wang, et al.	

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	70.	US- 4,761,799	08-02-1988	Arragon	
	71.	US- 4,764,846	08-16-1988	Go	
	72.	US- 4,770,640	09-13-1988	Walter	
	73.	US- 4,775,931	10-04-1988	Dickie, et al.	
	74.	US- 4,779,089	10-18-1988	Theus	
	75.	US- 4,785,396	11-15-1988	Murphy, et al.	
	76.	US- 4,803,621	02-07-1989	Kelly	
	77.	US- 4,818,985	04-04-1989	Ikeda	
	78.	US- 4,825,416	04-25-1989	Tam, et al.	
	79.	US- 4,831,338	05-16-1989	Yamaguchi	
	80.	US- 4,835,674	05-30-1989	Collins, et al.	
	81.	US- 4,837,682	06-06-1989	Culler	
	82.	US- 4,849,965	07-18-1989	Chomel, et al.	
	83.	US- 4,853,896	08-01-1989	Yamaguchi	
	84.	US- 4,858,112	08-15-1989	Puerzer, et al.	
	85.	US- 4,862,158	08-29-1989	Keller, et al.	
	86.	US- 4,870,622	09-26-1989	Aria, et al.	
	87.	US- 4,870,652	09-26-1989	Thornton	
	88.	US- 4,875,192	10-17-1989	Matsumoto	
	89.	US- 4,882,669	11-21-1989	Miura, et al.	
	90.	US- 4,891,791	01-02-1990	Iijima	
	91.	US- 4,920,486	04-24-1990	Nielson	
	92.	US- 4,926,385	05-15-1990	Fujishima, et al.	

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	93.	US- 4,933,835	06-12-1990	Sachs, et al.	
	94.	US- 4,937,733	06-26-1990	Gillett, Jr., et al.	
	95.	US- 4,939,510	07-03-1990	Masheff, et al.	
	96.	US- 4,940,909	07-10-1990	Mulder, et al.	
	97.	US- 4,945,471	07-31-1990	Neches	
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	99.	US- 4,947,484	08-07-1990	Twitty, et al.	
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	102.	US- 4,965,792	10-23-1990	Yano	
	103.	US- 4,975,763	12-04-1990	Baudouin, et al.	
	104.	US- 4,982,400	01-01-1991	Ebersole	
	105.	US- 4,998,069	03-05-1991	Nguyen, et al.	
	106.	US- 5,009,481	04-23-1991	Kinoshita, et al.	
	107.	US- 5,012,408	04-30-1991	Conroy	
	108.	US- 5,023,488	06-11-1991	Gunning	
	109.	US- 5,034,964	07-23-1991	Khan, et al.	
	110.	US- 5,038,317	08-06-1991	Callan, et al.	
	111.	US- 5,038,320	08-06-1991	Heath, et al.	
	112.	US- 5,056,060	10-08-1991	Fitch, et al.	
	113.	US- 5,063,561	11-05-1991	Crandall, et al.	
	114.	US- 5,077,693	12-31-1991	Hardee, et al.	
	115.	US- 4,941,128	07-10-1990	Wada, et al.	

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	116.	US- 5,083,260	01-21-1992	Tsuchiya	
	117.	US- 5,083,296	01-21-1992	Hara, et al.	
	118.	US- 5,093,807	03-03-1992	Hashimoto, et al.	
	119.	US- 5,107,491	04-21-1992	Chew	
	120.	US- 5,111,423	05-05-1992	Kopec, Jr., et al.	
	121.	US- 5,111,464	05-05-1992	Farmwald, et al.	
	122.	US- 5,117,494	05-26-1992	Costes, et al.	
	123.	US- 5,121,382	06-09-1992	Yang, et al.	
	124.	US- 5,129,069	07-07-1992	Helm, et al.	
	125.	US- 5,142,376	08-25-1992	Ogura	
	126.	US- 5,175,831	12-29-1992	Kumar	
	127.	US- 5,175,835	12-29-1992	Beighe, et al.	
	128.	US- 5,179,670	01-12-1993	Farmwald, et al.	
	129.	US- 5,193,149	03-09-1993	Awiszio, et al.	
	130.	US- 5,193,193	03-09-1993	Iyer	
	131.	US- 5,193,199	03-09-1993	Dalrymple, et al.	
	132.	US- 5,220,673	06-15-1993	Dalrymple, et al.	
	133.	US- 5,226,009	07-06-1993	Arimoto	
	134.	US- 5,247,518	09-21-1993	Takiyasu, et al.	
	135.	US- 5,317,723	05-31-1994	Heap, et al.	
	136.	US- 5,371,892	12-06-1994	Petersen, et al.	
	137.	US- 5,390,149	02-14-1995	Vogley, et al.	
	138.	US- 5,452,420	09-19-1995	Engdahl, et al.	

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	139.	US- 5,513,327	04-30-1996	Farmwald, et al.	
	140.	US- 5,847,997	12-08-1998	Harada, et al.	
	141.	US- 6,032,214	02-29-2000	Farmwald, et al.	
	142.	US- 6,034,918	03-07-2000	Farmwald, et al.	
	143.	US- 6,038,195	03-14-2000	Farmwald, et al.	
	144.	US- 4,817,058	03-28-1989	Pinkham	
	145.	US- 4,805,198	02-14-1989	Stern, et al.	
	146.	US- 4,535,427	08-13-1985	Jiang	
	147.	US- 4,882,710	11-21-1989	Hashimoto, et al.	
	148.	US- 5,546,346	08-13-1996	Agata, et al.	
	149.	US- 4,629,909	12-16-1986	Cameron	
	150.	US- 5,142,637	08-25-1992	Harlin, et al.	
	151.	US- 4,607,173	08-19-1986	Knoedl, Jr.	
	152.	US- 4,445,204	04-24-1984	Nishiguchi	
	153.	US- 4,597,019	06-24-1986	Nishimoto, et al.	
	154.	US- 4,412,286	10-25-1983	O'Dowd	
	155.	US- 4,882,712	11-21-1989	Ohno, et al.	
	156.	US- 4,628,489	10-09-1986	Ong, et al.	
	157.	US- 4,481,572	11-06-1984	Oschner	
	158.	US- 5,590,086	12-31-1996	Park, et al.	
	159.	US- 5,835,956	11-10-1998	Park, et al.	
	160.	US- 4,338,569	07-06-1982	Petrich	
	161.	US- 3,967,206	06-29-1976	Roberson, et al.	

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*(use as many sheets as necessary)*

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**10/716,595**

**Filing Date**

**November 20, 2003**

**First Named Inventor**

**Michael Farnwald**

**Art Unit**

2827

**Examiner Name**

**Tan Nguyen**

**Sheet**

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**Attorney Docket Number**

**57941.000062**

**U.S. PATENT DOCUMENTS**

\*Examiner  
Initials

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DOCUMENT NUMBER  
Number - Kind Code (if known)

Publication Date  
MM-DD-YYYYName of Patentee or  
Applicant of Cited Document

Pages, Columns, Lines,  
Where Relevant Passages or  
Relevant Figures Appear

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US- 4,520,465

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Sood

163.

US- 4,405,996

09-20-1983

Stewart

164.

US-	4,916,670
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04-10-1990

Suzuki

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		<b>Filing Date</b>	<b>November 20, 2003</b>
		<b>First Named Inventor</b>	<b>Michael Farmwald</b>
		<b>Art Unit</b>	<b>2827</b>
		<b>Examiner Name</b>	<b>Tan Nguyen</b>
<b>Sheet</b>	<b>9 of 18</b>	<b>Attorney Docket Number</b>	<b>57941.000062</b>

**FOREIGN PATENT DOCUMENTS**

*Examiner Initial	Cite No.	FOREIGN PATENT DOCUMENT		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	TRANSLATION	
		Country Code Number-Kind Code (if known)					YES	NO
	165.	JP	S56-047996	04-30-1981	Yoshida		<input type="checkbox"/>	<input type="checkbox"/>
	166.	EP	0 339 224	11-02-1989	Bowater, et al.		<input type="checkbox"/>	<input type="checkbox"/>
	167.	GB	2 201 569	09-01-1988	Currie		<input type="checkbox"/>	<input type="checkbox"/>
	168.	JP	S62-51387	03-06-1987	Hirahata, et al.		<input type="checkbox"/>	<input type="checkbox"/>
	169.	JP	S63-244389	10-11-1988	Horiguchi		<input type="checkbox"/>	<input type="checkbox"/>
	170.	JP	S57-210495	12-24-1982	Inagaki		<input type="checkbox"/>	<input type="checkbox"/>
	171.	JP	H03-076094	04-02-1991	Ishikawa		<input type="checkbox"/>	<input type="checkbox"/>
	172.	DE	37 42 487	07-07-1988	Kawai, et al.		<input type="checkbox"/>	<input type="checkbox"/>
	173.	JP	01-284132	11-15-1989	Kosugi, et al.		<input type="checkbox"/>	<input type="checkbox"/>
	174.	WO	89/06013	06-29-1989	Litaize, et al.		<input type="checkbox"/>	<input type="checkbox"/>
	175.	JP	H1-271861	10-30-1989	Shirae		<input type="checkbox"/>	<input type="checkbox"/>
	176.	JP	J1-232597	09-18-1989	Suzuki		<input type="checkbox"/>	<input type="checkbox"/>
	177.	JP	62-51093	03-05-1987	Takashi, et al.		<input type="checkbox"/>	<input type="checkbox"/>
	178.	JP	S61-220193	09-30-1986	Tetsuo		<input type="checkbox"/>	<input type="checkbox"/>
	179.	EP	1 640 847	03-29-2006	Farmwald		<input type="checkbox"/>	<input type="checkbox"/>
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<b>Sheet</b>	10 of 18	<b>Attorney Docket Number</b>	57941.000062

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			YES	NO
	180.	"High Speed CMOS Databook", Integrated Device Technology Inc., Santa Clara, CA, pg. 9-1 to 9-14, 1988.	<input type="checkbox"/>	<input type="checkbox"/>
	181.	A. Agarwal, et al., "An Analytical Cache Model", ACM Trans. on Comp. Sys., Vol. 7, No. 2, pg. 184-215, May 1989.	<input type="checkbox"/>	<input type="checkbox"/>
	182.	A. Agarwal, et al., "An Evaluation of Directory Scemes for Cache Conference", IEEE, 15 <sup>th</sup> Intern Symp. Comp. Architecture, pg. 280-289, June 1988.	<input type="checkbox"/>	<input type="checkbox"/>
	183.	A. Khan, "What's the Best Way to Minimize Memory Traffic", High Performance Systems, pg. 59-67, September 1989.	<input type="checkbox"/>	<input type="checkbox"/>
	184.	B. Wooley, et al., "Active Substrate System Integration", IEEE, Proceedings 1987 IEEE International Conference on Computer Design: VLSI in Computers & Processors, Rye Brook, New York, October 5, 1987.	<input type="checkbox"/>	<input type="checkbox"/>
	185.	Takai, et al., "250 Mbyte/sec Synchronous DRAM Using a 3-Stage Pipelined Architecture", 1993 Symposium on VLSI Circuits, Digest of Technical Papers, pg. 59-60, May 19-21, 1993.	<input type="checkbox"/>	<input type="checkbox"/>
	186.	Beresford, "How to Tame High Speed Design", High-Performance Systems, pg. 78-83, September 1989.	<input type="checkbox"/>	<input type="checkbox"/>
	187.	Boysel, et al., "Four-Phase LSI Logic Offers New Approach to Computer Designer", Four-Phase Systems Inc. Cupertino, CA, Computer Design, April 1970, pg. 141-146.	<input type="checkbox"/>	<input type="checkbox"/>
	188.	Boysel, et al., "Random Access MOS Memory Packs More Bits to the Chip", Electronics, February 16, 1970, pg. 109-146.	<input type="checkbox"/>	<input type="checkbox"/>
	189.	D. Hawley, "Superfast Bus Supports Sophisticated Transactions", High Performance Systems, pg. 90-94, September 1989. E. Davidson, "Electrical Design of a High Speed Computer Package", IBM J. Res. Develop., Vol. 26, No. 3, pg. 349-361, May 1982.	<input type="checkbox"/>	<input type="checkbox"/>
	190.	E. Davidson, "Electrical Design of a High Speed Computer Package", IBM J. Res. Develop., Vol. 26, No. 3, pg. 349-361, May 1982.	<input type="checkbox"/>	<input type="checkbox"/>

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			YES	NO
	191.	F. Hart, "Multiple Chips Speed CPU Subsystems", High-Performance Systems, Pg. 46-55, September 1989.	<input type="checkbox"/>	<input type="checkbox"/>
	192.	G. Chesley, "Virtual Memory Integration", Submitted to IEETC, September 1983.	<input type="checkbox"/>	<input type="checkbox"/>
	193.	G. L. Dix, et al., "Common Chips for Use in Disk and Diskette Controllers", IBM J. Res. Develop., Vol. 26, No. 4, July 1982, pg. 440-445.	<input type="checkbox"/>	<input type="checkbox"/>
	194.	Grover, et al., "Precision Time-Transfer in Transport Networks Using Digital Crossconnect Systems", IEEE Paper 47.2 Globecom, 1988, pg. 1544-1548.	<input type="checkbox"/>	<input type="checkbox"/>
	195.	H. Schumacher, "CMOS Subnanosecond True-ECL Output Buffer", IEEE Journal of Solid-State Circuits, Vol. 25, No. 1, pg. 150-154, February 1990.	<input type="checkbox"/>	<input type="checkbox"/>
	196.	Hansen, et al., "A RISC Microprocessor with Integral MMU and Cache Interface", MIPS Computer Systems, Sunnyvale, CA, IEEE 1986, pg. 145-148.	<input type="checkbox"/>	<input type="checkbox"/>
	197.	International Search Report dated July 8, 1991 for PCT Patent Application No. PCT/US91/0250 filed April 16, 1991.	<input type="checkbox"/>	<input type="checkbox"/>
	198.	J. Carson, et al., "Advanced On-Focal Plane Signal Processing for Non-Planar Infrared Mosaics", SPIE, Vol. 311, pg. 53-58, 1981.	<input type="checkbox"/>	<input type="checkbox"/>
	199.	J. Chun, et al., "A 1.2ns GaAs 4K Read Only Memory", IEEE Gallium Arsenide Integrated Circuit Symposium Technical Digest, pg. 83-86, November 1988.	<input type="checkbox"/>	<input type="checkbox"/>
	200.	J. Frisone, "A Classification for Serial Loop Data Communications Systems", Raleigh Patent Operations, November 2, 1972.	<input type="checkbox"/>	<input type="checkbox"/>
	201.	J. Peterson, "System-Level Concerns Set Performance Gains", High-Performance Systems, pg. 71-77, September 1989.	<input type="checkbox"/>	<input type="checkbox"/>

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			YES	NO
	202.	J. Sonntag, et al., "A Monolithic CMOS 10MHz DPLL for Burst-Mode Data Retiming", IEEE Interntaional Solid-State Circuits Conference (ISSCC), February 16, 1990.	<input type="checkbox"/>	<input type="checkbox"/>
	203.	Knut Alnes, "Scalable Coherent Interface", SCI--Fweb.89--doc52, (To Appear in Eurobus Conference Proceedings May 1989, pg. 1-8.	<input type="checkbox"/>	<input type="checkbox"/>
	204.	Knut Alnes, "SCI: A proposal for SCI Operation", SCI--Jan. 6, 1989--doc31, Norsk Data, Oslo, Norway, pg. 1-24, January 6, 1989.	<input type="checkbox"/>	<input type="checkbox"/>
	205.	M.Bazes, et al., "A Programmable NMOS DRAM Controller for Microcomputer Systems with Dual-Port Memory and Error Checking and Correction", IEEE Journal of Solid State Circuits, Vol. SC-18, No. 2, pg. 164-172, April 1983.	<input type="checkbox"/>	<input type="checkbox"/>
	206.	Moussouris, et al., "A CMOS Processor with Integrated Systems Functions", MIPS Computer Systems, Sunnyvale, CA, IEEE 1986, pg. 126-130.	<input type="checkbox"/>	<input type="checkbox"/>
	207.	Moussouris, J., "The Advanced Systems Outlook-Life Beyond RISC: The Next 30 Years in High-Performance Computing", Computer Letter, July 31, 1989 (an edited excerpt from an address at the fourth annual conference on the Advanced Systems Outlook, in San Francisco, CA (June 5)).	<input type="checkbox"/>	<input type="checkbox"/>
	208.	N. Margulis, "Single Chip RISC CPU Eases Single Chip System Design", High Performance Systems, pg. 34-36, 40-41, and 44, September 1989.	<input type="checkbox"/>	<input type="checkbox"/>
	209.	R. L. Schmidt, "A Memory Control Chip for Formatting Data into Block Sutable for Video Coding Applications", IEEE Transactions on Circuits and Systems, Vol. 36, No. 10, pg. 1275-1280, October 1989.	<input type="checkbox"/>	<input type="checkbox"/>
	210.	R. Matick, "Comparison of Memory Chip Organizations vs. Reliability in Virtual Memories", FTCS 12 <sup>th</sup> Annual International Symposium Fault-Tolerent Committee, pg. 223-227, June 22, 1984.	<input type="checkbox"/>	<input type="checkbox"/>
	211.	R. Pease, et al., "Physical Limits to the Useful Packaging Density of Electronic Systems", Standard Center for Integrated Systems, Stanford University, September 1988.	<input type="checkbox"/>	<input type="checkbox"/>

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		<b>First Named Inventor</b> <b>Michael Farnwald</b>	<b>Art Unit</b> <b>2827</b>
		<b>Examiner Name</b> <b>Tan Nguyen</b>	
		<b>Attorney Docket Number</b> <b>57941.000062</b>	
<b>Sheet</b>	<b>13 of 18</b>		

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			YES	NO
	212.	T. Riordan, "MIPS R2000 Processor Interface 78-00005(C)", MIPS Computer Systems, Sunnyvale, CA, June 30, 1987,pg. 1-83.	<input type="checkbox"/>	<input type="checkbox"/>
	213.	S. Kwon, et al., "Memory Chip Organizations for Improved Reliability in Virtual Memories" IBM Technical Disclosure Bulletin, Vol. 25, No. 6, pg. 2952-2957, Nov. 1982.	<input type="checkbox"/>	<input type="checkbox"/>
	214.	S. Watanabe, et al., "An Experimental 16Mbit Cmos Dram Chip with a 100-MHz Serial Read/Write Mode", IEEE Journal of Solid State Circuits, Vol. 24, No. 3, pg. 763-770, June 1982.	<input type="checkbox"/>	<input type="checkbox"/>
	215.	T. Yang, et al., "A 4-ns 4Kx1-bit Two-Port BiCMOS SRAM", IEEE Journal of Solid-State Circuits, Vol. 23, No. 5, pg. 1030-1040, October 1988.	<input type="checkbox"/>	<input type="checkbox"/>
	216.	European Search Report dated April 13, 2006 for European Patent Application No. 05026720.2 filed April 16, 1991.	<input type="checkbox"/>	<input type="checkbox"/>
	217.	Saito, Shozo; Fujii, Syuso; Okoda, Yoshio; Sawada, Shizuo; Shinozaki, Satoshi; Natori, Kenji; Ozawa, Osamu, "A 1-Mbit CMOS DRAM with Fast Page Mode and Static Column Mode," IEEE Journal of Solid-State Circuits, Vol. SC-20, No. 5 (Oct 1985), pp. 903-908.	<input type="checkbox"/>	<input type="checkbox"/>
	218.	Fuji, Syuso; Ogihara, Masaki; Shimizu, Mitsuru; Yoshida, Munehiro; Numata, Kenji; Hara, Takahiko; Watanabe, Shigeyoshi; Sawada, Shizuo; Mizuno, Tomohisa; Kumagi, Junpei; Yoshikawa, Susumu; Kaki, Seiji; Saito, Yoshikazu; Aochi, Hideaki; Hamamot, Takeshi; Toita, Koichi, "A 45-ns 16-Mbit DRAM with Triple-Well Structure," IEEE Journal of Solid-State Circuits, Vol. 24, No. 5 (Oct 1989), pp. 1170-1175.	<input type="checkbox"/>	<input type="checkbox"/>
	219.	Martino, William L. Jr.; Moench, Jerry D.; Bormann, Alan R.; Tesch, Rodney C., "An On-Chip Back-Bias Generator for MOS Dynamic Memory," IEEE Journal of Solid-State Circuits, Vol. SC-15, No. 5 (Oct 1980), pp. 820-826.	<input type="checkbox"/>	<input type="checkbox"/>
	220.	Intel iAPX43202 VLSI Interface Processor Data Sheet, Intel Publication Number 171874-001 Rev. A (Intel, 1981).	<input type="checkbox"/>	<input type="checkbox"/>
	221.	Baba, Fumio, Mochizuki, Hirohiko; Yabu, Takashi; Shirai, Kazunari; Miyasaka, Kiyoshi, "A 64-K DRAM with 35 ns Static Column Operation," IEEE Journal of Solid-State Circuits, Vol. SC-18, No. 5, (Oct 1983), pp. 447-451.	<input type="checkbox"/>	<input type="checkbox"/>

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<b>Sheet</b>	14 of 18	<b>Attorney Docket Number</b>	57941.000062

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			YES	NO
	222.	Miyamoto, Hiroshi; Yamagata, Tadato; Mori, Shigeru; Aono, Tetsuya; Ogoh, Ikuo; Yamada, Michihiro, "Improved Address Buffers, TTL Input Current Reduction, and Hidden Refresh Test Mode in a 4-Mb Dram," IEEE Journal of Solid-State Circuits, Vol. 25, No. 2 (April 1990), pp. 525-574.	<input type="checkbox"/>	<input type="checkbox"/>
	223.	Ahlquist, C. Norman; Breivogel, Joseph R.; Koo, James T.; McCollum, John L.; Oldham, William g.; Renninger, Alan L., "A 16 384-Bit Dynamic Ram," IEEE Journal of Solid-State Circuits, Vol. SC-11, No. 5 (Oct 1976), pp. 570-573.	<input type="checkbox"/>	<input type="checkbox"/>
	224.	Takashima, Daisaburo; Watanabe, Shigeyoshi; Fuse, Tsuneaki; Sunouchi, Kazumasa; Hara, Takahiko, "Low-Power On-Chip Supply Voltage Conversion Scheme for Ultrahigh-Density DRAM's," IEEE Journal of Solid-State Circuits, Vol. 28, No. 4 (April 1993), pp. 504-509.	<input type="checkbox"/>	<input type="checkbox"/>
	225.	Natori, Kenji; Ogura, Mitsugi; Iwai, Hiroshi; Maeguchi, Kenji; Taguchi, Shinji, "A 64 kbit MOS Dynamic Random Access Memory," IEEE Journal of Solid-State Circuits, Vol. SC-14, No. 2 (April 1979), pp. 482-485	<input type="checkbox"/>	<input type="checkbox"/>
	226.	Kalter, Howard L.; Coppens, Pierre D.; Ellis, Wayne F.; Fifield, John A; Kokoszka, Daryl J.; Leasure, Terry L.; Miller, Christopher P.; Nguyen, Quan; Papritz, Ronald E.; Patton, Charles S.; Poplawski, J. Michael; Tomashot, Steven W.; Van Der Hoeven, Willem B., "An Experimental 80-ns 1-Mbit DRAM with Fast Page Operation," IEEE Journal of Solid-State Circuits, Vol. SC-20, No. 5 (Oct 1985), pp. 914-923	<input type="checkbox"/>	<input type="checkbox"/>
	227.	Kawahara, Takayuki; Kawajiri, Yoshiki; Horiguchi, Masahi; Akiba, Takesada; Kitsukawa, Goro; Kure, Tokuo; Aoki, Masakazu, "A Charge Recycle Refresh for Gb-Scale DRAM's in File Applications," IEEE Journal of Solid-State Circuits, Vol. 29 (June 1994), pp. 715-722.	<input type="checkbox"/>	<input type="checkbox"/>
	228.	Kushiyama, Natsuki; Watanabe, Yohi; Ohsawa, Takashi; Muraoka, Kazuyoshi; Nagahama, Yousei; Furuyama, Tohru, "A 12-MHz Data Cycle 4-Mb DRAM with Pipeline Operation," IEEE Journal of Solid-State Circuits, Vol. 26, No. 4 (April 1991), pp. 479-483.	<input type="checkbox"/>	<input type="checkbox"/>
	229.	Miyamoto, Hiroshi; Yamagata, Tadato; Mori, Shigeru; Kobayashi, Toshifumi; Satoh, Shin-ichi; Yamada, Michihiro, "A Fast 256K x4 CMOS DRAM with a Distributed Sense and Unique Restore Circuit," IEEE Journal of Solid-State Circuits, Vol. SC-22, No. 5 (Oct 1987), pp. 861-867.	<input type="checkbox"/>	<input type="checkbox"/>
	230.	Fuji, Syuso; Natori, Kenji; Furuyama, Tohru; Daito, Shozo; Toda, Haruki; Tanaka, Takeshi; Ozawa, Osamu, "A Low-Power Sub 100 ns 256K Bit Dynamic RAM," IEEE Journal of Solid-State Circuits, Vol. SC-18, No. 5 (Oct 1983), pp. 441-446.	<input type="checkbox"/>	<input type="checkbox"/>

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	231.	Lu, Nicky C.C.; Chao, Hu H.; Hwang, Wei; Henkels, Walter H.; Rajeevakumar, T.V.; Hanafi, Hussein I.; Terman, Lewis M.; Franch, Robert L., "A 20-ns 128-kbit X 4 High-Speed DRAM with 330-Mbit/s Data Rate," IEEE Journal of Solid-State Circuits, Vol. 23, No. 5 (Oct 1988), pp. 1140-1149.	<input type="checkbox"/>	<input type="checkbox"/>
	232.	P1596: SCI, A Scalable Coherent Interface Bus Specification Components (Nov 18, 1988).	<input type="checkbox"/>	<input type="checkbox"/>
	233.	Choi, et al., "16Mbit Synchronous DRAM with 125Mbyte/sec Data Rate", 1993 Symposium on VLSI Circuits, Digest of Technical Papers, pg. 65-66, 1993.	<input type="checkbox"/>	<input type="checkbox"/>
	234.	Ebel, et al., "A 4096-Bit High-Speed Emitter-Coupled-Logic (ECL) Compatible Random-Access Memory" IEEE Journal of Solid-State Circuits, Vol. SC-10, No.5, pg. 262-267, October 1976.	<input type="checkbox"/>	<input type="checkbox"/>
	235.	Fujiwara, et al., "A200MHz 16Mbit Synchronous DRAM with Block Access Mode", 1994 Symposium on VLSI Circuits Digest of Technical Papers, pg. 79-80, 1994.	<input type="checkbox"/>	<input type="checkbox"/>
	236.	Hatakeyama, et al., "TP 4.5: A256Mb SDRAM Using a Register-Controlled Digital DLL, IEEE ISSCC Digest of Technical Papers, February 6-8, 1997.	<input type="checkbox"/>	<input type="checkbox"/>
	237.	Intel, "refers to: iAPX432 IP Datasheet, iAPX432 GDP Datasheet, iAPX432 Manual, IAPX432 Specification (BIU), iAPX432 Specification (MCU)", 1981-1983.	<input type="checkbox"/>	<input type="checkbox"/>
	238.	Intel, "Intel iAPX432 Interconnect Architecture Reference Manual", Intel Publication No. 172487-001, December 1982.	<input type="checkbox"/>	<input type="checkbox"/>
	239.	IBM, "Range Check of an Address Counter", IBM Technical Disclosure Bulletin, pg. 2136-2137, December 1973.	<input type="checkbox"/>	<input type="checkbox"/>

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			YES	NO
	240.	"IEEE Standard for a Simple 32-Bit Backplane Bus", ANSI/IEEE Std., pg. 1193-1987, February 24, 1988.	<input type="checkbox"/>	<input type="checkbox"/>
	241.	"IEEE Standard for High-Bandwidth Memory Interface Based on Scalable Coherent Interface (SCI) Signaling Technology", IEEE Std., pg. 1596.4-1996, September 15, 1996.	<input type="checkbox"/>	<input type="checkbox"/>
	242.	"IEEE Standard for scalable Coherent Interface (SCI)", IEEE Std. 1596-1992, August 2, 1993.	<input type="checkbox"/>	<input type="checkbox"/>
	243.	"Double Data Rate (DDR) SDRAM Specification", JEDEC Standard-JESD79D, January 2004.	<input type="checkbox"/>	<input type="checkbox"/>
	244.	Llewellyn, et al., "WAM 1.1: A33Mb/s Data Synchronizing Phase-Locked-Loop Circuit", IEEE ISSCC Digest of Technical Papers, 1988, pg. 12-13, 276-277, February 17, 1988.	<input type="checkbox"/>	<input type="checkbox"/>
	245.	Lu, et al., "A Novel CMOS Implementation of Double-Edge-Triggered Flip-Flops", IEEE Journal of Solid-State Circuits, Vol. 25, No. 4, pg. 1008-1010, August 1990.	<input type="checkbox"/>	<input type="checkbox"/>
	246.	MacDonald, et al., "FAM 16.2: 200Mb Wafer Memory", IEEE IssCC, Digest of Technical Papers, 1989, pg. 240-241, 350, February 17, 1989.	<input type="checkbox"/>	<input type="checkbox"/>
	247.	McGeedy, "The i960CA SuperScalar Implementation of the 80960 Architecture", 1990 COMPCON Proceedings, pg. 232-240, 1990.	<input type="checkbox"/>	<input type="checkbox"/>
	248.	Thorson, et al., "ECL Bus Controller Hits 266 Mbytes/s", Microprocessor Report, Vol. 4, No. 1, pg. 12-14, January 24, 1990.	<input type="checkbox"/>	<input type="checkbox"/>
<b>EXAMINER SIGNATURE</b>		<b>DATE CONSIDERED</b>		
<p><b>*EXAMINER:</b> Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.</p>				

Substitute for form 1449/PTO  <div style="text-align: center;"><b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b></div> <div style="text-align: center;"><i>(use as many sheets as necessary)</i></div>		<b>Application Number</b>	10/716,595
		<b>Filing Date</b>	November 20, 2003
		<b>First Named Inventor</b>	Michael Farnwald
		<b>Art Unit</b>	2827
		<b>Examiner Name</b>	Tan Nguyen
<b>Sheet</b>	17 of 18	<b>Attorney Docket Number</b>	57941.000062

**OTHER DOCUMENTS - NON-PATENT LITERATURE DOCUMENTS**

*Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	TRANSLATION	
			YES	NO
	249.	Nitta, et al., "SP 23.5: 1.6 GB/s Data-Rate 1 Gb Synchronous DRAM with Hierarchical Square-Shaped Memory Block and Distributed Bank Architecture", IEEE ISSCC Digest of Technical Papers, pg. 376-377, 477, February 10, 1996.	<input type="checkbox"/>	<input type="checkbox"/>
	250.	Pelgrom, et al., "A 32-kbit Variable-Length Shift Register for Digital Audio Application", IEEE Journal of Solid-State Circuits, Vol. SC-22, No. 3, pg. 415-422, June 1987.	<input type="checkbox"/>	<input type="checkbox"/>
	251.	Rau, et al., "The Cydra 5 Departmental Supercomputer Design Philosophies, Decisions, and Trade-offs", IEEE Computer, pg. 12-35, January 1989.	<input type="checkbox"/>	<input type="checkbox"/>
	252.	Saeki, et al., "SP 23.4: A 2.5 ns Clock Access 250MHz 256Mb SDRAM with a Synchronous Mirror Delay", IEEE ISSCC Digest of Technical Papers, pg. 374-375, 476, February 10, 1996.	<input type="checkbox"/>	<input type="checkbox"/>
	253.	UNISYS, "UNISYS Configurable DRAM Proposal", JEDEC 42.3 Meeting Minutes, December 16, 1988.	<input type="checkbox"/>	<input type="checkbox"/>
	254.	Bakka, et al., "SCI: Logical Level Proposals - Working Paper", January 6, 1989.	<input type="checkbox"/>	<input type="checkbox"/>
	255.	Kristiansen, et al., "Scalable Coherent Interface, February 1989.	<input type="checkbox"/>	<input type="checkbox"/>
	256.	Watanabe, et al., "A New CR-Delay Circuit Technology for High-Density and High-Speed DRAM's", IEEE Journal of Solid-State Circuits, Vol. 24, No. 4, pg. 905-910, August 1989.	<input type="checkbox"/>	<input type="checkbox"/>
	257.	Yoo, et al., "A 150 MHZ 8-Bank 256M Synchronous DRAM with Wave Pipelining Methods", IEEE ISSCC Digest of Technical Papers, pg. 250-251, 374, February 17, 1995.	<input type="checkbox"/>	<input type="checkbox"/>

<b>EXAMINER SIGNATURE</b>	<b>DATE CONSIDERED</b>
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		<b>Examiner Name</b>	<b>Tan Nguyen</b>
<b>Sheet</b>	<b>18 of 18</b>	<b>Attorney Docket Number</b>	<b>57941.000062</b>

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			YES	NO
	258.	European Search Report dated March 23, 2006 for European Patent No. 1 640 847, published May 31, 2006.	<input type="checkbox"/>	<input type="checkbox"/>
			<input type="checkbox"/>	<input type="checkbox"/>
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